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Publisher: Taylor & Francis  
Informa Ltd Registered in England and Wales Registered Number: 1072954  
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## International Journal of Production Research

Publication details, including instructions for authors and subscription information:  
<http://www.informaworld.com/smpp/title~content=t713696255>

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First Published: July 2008

To cite this Article: Bahaji, N. and Kuhl, M. E. (2008) 'A simulation study of new multi-objective composite dispatching rules, CONWIP, and push lot release in semiconductor fabrication', International Journal of Production Research, 46:14, 3801 — 3824

To link to this article: DOI: 10.1080/00207540600711879

URL: <http://dx.doi.org/10.1080/00207540600711879>

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## **A simulation study of new multi-objective composite dispatching rules, CONWIP, and push lot release in semiconductor fabrication**

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*(Revision received March 2006)*

This paper evaluates dispatching rules and order release policies in two wafer fabrication facilities (thereafter referred to as 'fab') representing ASIC (application specific integrated circuit) and low-mix high-volume production. Order release policies were fixed-interval (push) release, and constant work-in-process (CONWIP) (pull) policy. Following rigorous fab modelling and statistical analysis, new composite dispatching rules were found to be robust for average and variance of flow time, as well as due-date adherence measures, in both production modes.

*Keywords:* Scheduling; Simulation; Dispatching rules; Semiconductor manufacturing

### **1. Introduction**

The success of a semiconductor manufacturer is determined by its ability to provide the quantity and quality demanded by customers in an extremely competitive environment. Although changes in technology such as larger wafer sizes and smaller chips have enhanced productivity, the highly complex nature of semiconductor manufacturing, if not managed properly, can result in high levels of work-in-process (WIP), long flow (cycle) times, and poor due-date performance. The concept of shop floor control addresses these issues by implementing strategies with the goal of maximising fab productivity, as defined by faster flow times, lower WIP levels, and better due date adherence.

This paper addresses two main aspects of shop floor control: dispatching rules and lot release strategies. The goals of this study are to:

- (a) Identify current benchmark and high-claim dispatching rules and commonly used lot release strategies from the literature.
- (b) Develop new composite dispatching rules.
- (c) Conduct a rigorous experimental performance evaluation using simulation to quantitatively compare the effect of the combination of dispatching rules and lot release strategies on key fab performance measures.

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Table 1. List of acronyms.

Abbreviation	Description
AT	Arrival Time (Shop Floor)
ATStep	Arrival Time (Processing Step)
ASIC	Application Specific Integrated Circuit
CI	Confidence Interval
CONWIP	CONstant Work IN Process
CR	Critical Ratio
DR	Dispatching Rule
EDD	Earliest Due Date
ESD	Earliest Start Date
FCFS	First Come First Serve
HXF	Highest X Factor
LWNQ	Least Work in Next Queue
MBS	Minimum Batch Size
MCP	Mean Comparison Procedure
MCT	Mean Conditional Tardiness
MFT	Mean Flow Time
MRP	Material Requirements Planning
MRP II	Manufacturing Resources Planning
NP	Number of Products
OR	Order Release
PT	Processing Time
RPT	Remaining Processing Time
RR	Raghu & Rajendran's (Dispatching Rule)
SDFT	Standard Deviation of Flow Time
SPT	Shortest Processing Time
SRPT	Shortest Remaining Processing Time
TIS	Time in the System
WINQ	Work in Next Queue
WIP	Work in Process
Wt	Weighted
XF	X Factor (or 'multiplier of theoretical processing time')

(d) Identify robust combinations of the shop floor control strategies in ASIC (make-to-order) and low-mix high-volume (make-to-stock) fabs.

The rest of the paper is organised as follows. Section 2 sets the background for shop floor control strategies. Section 3 summarises previous studies involving dispatching rules and lot release strategies. The experimental performance evaluation and the results are presented in sections 4 and 5, respectively. Finally, the conclusions of this research are presented in section 6. A list of helpful acronyms is initially provided in table 1.

## 2. Background

### 2.1 Scheduling vs dynamic shop floor control

It is crucial to initially make a broad distinction between scheduling in its traditional (and mostly-static) sense, and the narrower area of dynamic shop floor control.

Scheduling is concerned with ‘the allocation of resources over time to perform tasks’ (MacCarthy and Liu 1993). Its approach is to determine well in advance the exact sequencing and timing of job-starts. Typically, while key decision variables such as demand patterns and manufacturing lead times are kept static in the planning horizon, a fixed number of  $n$  jobs are to be processed by  $m$  machines; given a set of constraints, and with the goal of optimising a certain performance measure.

In contrast, dynamic shop floor control, with its two components of input regulation and dispatching, mostly relies on heuristics in order to decide ‘how much material to start into the facility, and how to control the material once started’ (Uzsoy *et al.* 1992). Static scheduling approaches are thus more appropriate for setting long-term aggregate goals, rather than the ongoing hourly challenges of shop floor control. Finally, since many of the mathematical programming methods associated with scheduling are inefficient for the combined computational complexity of the performance measures *and* system variables of semiconductor manufacturing, discrete event simulation is useful in evaluating the merit of dynamic shop floor strategies.

## 2.2 Fab performance measures

Wafer fabrication is characterised by unreliable tools, re-entrant WIP flow, shifting bottlenecks, mixed batching modes, sequence-dependent set-ups, variable flow times, and a mix of flow-line and job-shop aspects (Bahaji 2000, Fowler *et al.* 2002). Figure 1 illustrates the two major classes of fab performance measures at stake. Job-oriented measures such as tardiness are due-date dependent, while shop-oriented ones like flow time ( $W$ ), also known as cycle time, WIP level ( $L$ ), and throughput rate ( $\lambda$ ) are interrelated via Little’s law (Little 1961):  $L = \lambda W$ .

Given that  $\lambda$  is either the input or bottleneck rate, flow time is proportional to WIP. WIP not only balances the benefits of buffering with inventory costs, risks of congestion, late deliveries, and product obsolescence (Graves and Milne 1997); it is also key for market responsiveness, and for reducing yield loss due to particle exposure. Further, in the fab context, contrary to typical job-shop scheduling, due-date based measures such as tardiness, are secondary to Little’s law system-oriented ones, especially flow time and WIP level. In fact ‘98% cycle time’, which is semiconductor industry jargon for a performance measure defined as the mean plus

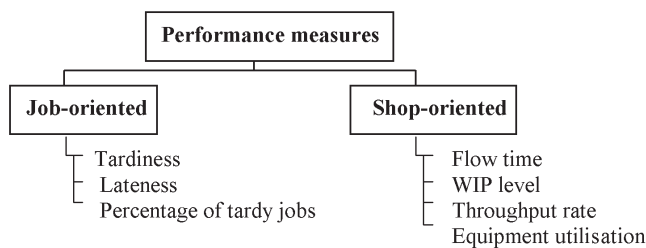


Figure 1. Major classes of performance measures.

three standard deviations of flow time, is used as an alternative predictor of due-date adherence (Sandell and Srinivasan 1996). Note that '98% cycle time' should not be confused with the 98th percentile of flow time.

### 2.3 Dynamic shop floor control

**2.3.1 Input regulation.** Whether of the 'push' or 'pull' type, input regulation (also called order release control; see Fowler *et al.* 2002 for a survey) or targets 'shorter, more reliable flow times by releasing work to the shop in a controlled manner' (Uzsoy *et al.* 1994). Material requirements planning (MRP) and manufacturing resources planning (MRP II) illustrate push policies; where lots are released in fixed intervals, based on static demand and lead time estimates; and regardless of floor congestion (Gstettner and Kuhn 1996). Pull strategies, however, stress swift market response without excess inventory (Hopp and Spearman 1996), i.e. WIP is fixed by timing job starts with job completions. WIP can be set to a constant level at every processing stage (kanban systems), over the entire fab (CONWIP of Spearman *et al.* 1990), or up to the bottleneck machine (Goldratt and Fox 1986).

**2.3.2 Dispatching.** Dispatching rules dynamically rank queues by computing lot priority indices (Bhaskaran and Pinedo 1992). Rule effectiveness depends on the performance measure at stake, shop-load level, and due-date tightness (Kutanoglu and Sabuncuoglu 1999). Dispatching rules use lot and system attributes such as: arrival time, due date, processing time(s), queue length(s), work content, and setup time. Dispatching rule classification schemes are shown in figure 2. For example, 'simple dispatching rules' use one attribute; while 'composite dispatching rules' use the attributes' ratios, exponentiation, truncation, or conditional combinations. FCFS (first come first serve) is a simple rule based on arrival time. 'Scaling parameters' can also be used to weigh multiple objectives.

A review of key composite rule building blocks of processing time, arrival time, and due date is presented next. Processing time (PT) information targets mean flow time and throughput rate; but can also perform well for due-date measures, under heavy traffic and tight due-dates (Blackstone *et al.* 1982, Bhaskaran and Pinedo 1992, Raghu and Rajendran 1993, Kutanoglu and Sabuncuoglu 1999,

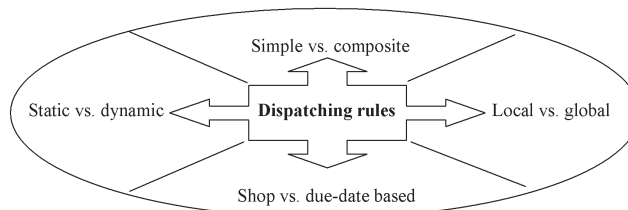


Figure 2. Four different schemes of classifying dispatching rules.

Rajendran and Holthaus 1999). Either the immediate or total remaining processing times can be used respectively in SPT (shortest processing time) and SRPT (shortest remaining processing time) rules, respectively. PT-based rules however, marginalise longer-processing products. Completed processing time is used in the multiplier of theoretical flow time rule, or X factor (XF) (Fowler *et al.* 1997), and describes accrued flow time as a multiple of its theoretical processing (non-queue) time. Arrival time (AT) refers to initial lot release time, while (ATStep) is the arrival time at a processing step. Time in the system (TIS), uses the dispatching decision time minus arrival time. Both AT and TIS reduce flow time variance (Holthaus and Rajendran 1997, Holthaus 1999). Work in the next queue (WINQ) adds all the lots' processing times in a given queue. It diverts WIP away from congested queues (Holthaus and Rajendran 1997 and Holthaus 1999). Finally, due-date attribute use, does not necessarily improve due-date adherence, and may hinder the all-important flow time and system throughput measures of the semiconductor context (Wein and Chevalier 1992).

### 3. Previous comparative studies

An in-depth review of flow control simulation studies is found in Bahaji (2000). Table 2 compares representative past works modelling the re-entrant flow common in semiconductor fabrication. In general, researchers have concluded that 'a significant amount of research remains to be done in measuring the effectiveness of dispatching rules' (Bhaskaran and Pinedo 1992) and that 'comprehensive testing of the previously developed [flow control] approaches in realistic settings' was needed (Fowler *et al.* 2002). Uzsoy *et al.* (1994) and Cigolini *et al.* (1998) also found that 'contradictory' results were common.

When looking at table 2, there are three aspects to keep in mind in order to appreciate the effort put forth in this study. The first is the test bed model used, and how it mirrors the complexity of actual semiconductor fabrication in terms of including factors such as re-entrant flow, batching, and set-up operations. The second is the comprehensiveness of the recorded performance measures, and the breath of the investigated independent design variables. Finally, semiconductor fab flow studies can benefit from job-shop scheduling literature findings. Consequently, this study compares some previous shop floor control strategies in a realistic fab model, while infusing dispatching rule design ideas from past job shop scheduling research. By reporting performance measures beyond the average and variance flow time, the attempt was also to mirror some trends of the job shop scheduling literature where due-date-based measures are commonplace.

### 4. Design of experiments

The experimental environment is summarised in table 3. Ample detail for this  $2 \times 2 \times 14$  full factorial experiment is found in Bahaji (2000).

Table 2. Fab modeling and recorded performance measures in selected past studies.

	Modeling & Flow Control Aspects											Performance Measures				
	# of Workstations if reentrant fab	Dispatching	Input regulation	X parallel stations per workstation	Multiple products	Due dates	Batch and set-up modeling	Operator modeling	Number-of-products factor	ANOVA	Mean comparison procedures	Software package	Mean flow time	Standard deviation of flow time	Percentage of tardy jobs	Mean tardiness or Mean conditional tardiness
Wein (1988)	24	✓	✓	✓							SIMAN	✓	✓			
Glassev and Resende (1988)	5-41	✓	✓	✓							FabSIM (UCB)					
Lu and Kumar (1991)	3	✓									SLAM II	✓	✓			
Wein and Chevalier (1992)	2	✓	✓		✓	✓					Unspecified			✓	✓	✓
Ehteshami <i>et al.</i> (1992)	13	✓		✓							BLOCS (UCB)	✓	✓			
Duenyas (1994)	2-3	✓	✓		✓						Unspecified	✓				
Lu <i>et al.</i> (1994)	12-24	✓	✓	✓		✓			✓	✓	Unspecified		✓			
Li <i>et al.</i> (1996)	4	✓					✓				Unspecified	✓	✓			
Sandell and Srinivasan (1996)	3-45		✓	✓					✓		Delphi & ManSIM	✓	✓			
Graves and Milne (1997)	-		✓								SIMAN	✓				
Palmeri and Collins (1997)	83	✓		✓	✓	✓					AutoSched 4.0	✓				
Kim <i>et al.</i> (1998)	24	✓	✓	✓		✓					FACTOR AIM	✓				✓
Mittler and Schoemig (1999)	73-83	✓		✓	✓	✓	✓				Delphi/FX	✓	✓			
Rose (2001)	103	✓		✓	✓	✓	✓				Factory Explorer 2	✓	✓			
Kim <i>et al.</i> (2003)	85	✓		✓	✓	✓	✓		✓		FACTOR AIM				✓	
Monch and Zimmermann (2004)	80	✓		✓	✓	✓	✓				AutoSched AP 7.1	✓			✓	
This study	85	✓	✓	✓	✓	✓	✓	✓	✓	✓	AutoSched AP 6.25	✓	✓	✓	✓	✓

#### 4.1 Experimental factors

**4.1.1 Dispatching rules.** Benchmark and past research priority indices are given following figure 3, which lists the notation used in the expressions.

$$FCFS_{inj} = \sigma_{inj} \quad (1)$$

$$ESD_{in} = \beta_{in} \quad (2)$$

$$EDD_{in} = d_{in} \quad (3)$$

$$LWNQ_{inj} = \omega_{in(j+1)} \quad (4)$$

$$CR_{inj} = \frac{d_{in} - t}{\sum_{q=j}^{m_n} p_{nq}} \quad (5)$$

Table 3. Summary of this study’s experimental factors.

Factor	Number of levels	Levels	Remarks
Number of products	2	3 products All 21 original products	Low-variety fab (make-to-market) ASIC fab (make-to-order)
Order release	2	CONWIP Push	Fixed-WIP Fixed-interval
Dispatching	14	FCFS CR EDD LWNQ ESD HXF CR + SPT AT-RPT PT/TIS (PT + WINQ)/TIS (PT + WINQJ)/XF (ATStep-RPT)/XF Wt(PT + WINQ)/XF Wt(ATStep-RPT)/XF	Benchmark Benchmark Benchmark Benchmark Benchmark Anderson and Nyirenda (1990) Holthaus (1999) & Lu <i>et al.</i> (1994) Holthaus (1999) Holthaus (1999) New/Proposed New/Proposed New/Proposed New/Proposed

*i* : Job (lot) index  
*j, q* : Operation (processing step) indices  
*n* : Product type index  
 $\alpha$  : Due-date tightness level  
 $\eta$  : Machine utilisation rate  
*d* : Due date  
*m* : Number of operations  
*p* : Processing time  
*t* : Time of the dispatching decision  
 $\beta$  : Shop floor arrival time  
 $\sigma$  : Operation arrival time  
 $\omega$  : Work content (sum of processing times of jobs in the queue)  
*W* : Estimated waiting time in next step

Figure 3. Priority index notation.

$$HXF_{inj} = \frac{1}{(t - \beta_{in}) / (\sum_{q=1}^j p_{nq})} \tag{6}$$

$$(AT - RPT)_{inj} = \beta_{in} - \sum_{q=j}^{m_n} p_{nq} \tag{7}$$

$$(CR + SPT)_{inj} = p_{nj} \cdot \max \left[ \frac{d_{in} - t}{\sum_{q=j}^{m_n} p_{nq}}, 1.0 \right] \tag{8}$$

$$(\text{PT} + \text{WINQ})/\text{TIS}_{inj} = \frac{p_{nj} + \omega_{in(j+1)}}{t - \beta_{in}} \quad (9)$$

$$(\text{PT}/\text{TIS})_{inj} = \frac{p_{nj}}{t - \beta_{in}}. \quad (10)$$

Our proposed rules are given as

$$(\text{PT} + \text{WINQ})/\text{XF}_{inj} = \frac{p_{nj} + \omega_{in(j+1)}}{(t - \beta_{in}) / \left( \sum_{q=1}^j p_{nq} \right)} \quad (11)$$

$$(\text{ATStep} - \text{RPT})/\text{XF}_{inj} = \frac{\sigma_{inj} - \sum_{q=j}^{m_n} p_{nq}}{(t - \beta_{in}) / \left( \sum_{q=1}^j p_{nq} \right)} \quad (12)$$

$$\begin{aligned} \text{Wt}(\text{PT} + \text{WINQ})/\text{XF}_{inj} = & \exp\left(-\frac{t - \beta_{in}}{\sum_{q=1}^j p_{nq}}\right) \cdot \left\{ \frac{p_{nj} + \omega_{in(j+1)}}{(t - \beta_{in}) / \left( \sum_{q=1}^j p_{nq} \right)} \right\} \\ & + \exp\left(\frac{t - \beta_{in}}{\sum_{q=1}^j p_{nq}}\right) \cdot \left\{ \frac{1}{(t - \beta_{in}) / \left( \sum_{q=1}^j p_{nq} \right)} \right\} \end{aligned} \quad (13)$$

$$\text{Wt}(\text{ATStep} - \text{RPT})/\text{XF}_{inj} = \left( \sigma_{inj} - \sum_{q=1}^j p_{nq} \right) \cdot \text{Wt}(\text{PT} + \text{WINQ})/\text{XF}_{inj} \quad (14)$$

Consulting the acronym definitions of table 1 will be helpful in understanding the rules listed above. Also note that since some priority indices are independent of the lot (or processing step), indices  $i$  and  $j$  are respectively omitted from some rule notations. It is also important to keep in mind that the first seven rules were reused as building blocks for the latter composite rules. Depending on which attribute needs to be minimised or maximised, summation and multiplication of attributes on the one hand, and subtraction and division, on the other, can be used.  $(\text{PT} + \text{WINQ})/\text{XF}$  and  $\text{Wt}(\text{PT} + \text{WINQ})/\text{XF}$  (equations 11 and 13) will be used as an illustration.  $(\text{PT} + \text{WINQ})/\text{XF}$  expedites lots with the least processing time (PT) and work in the next queue (WINQ) as shown in the numerator expression  $\text{PT} + \text{WINQ}$ . The same rule also prioritises lots with the greatest X factor quantity found in the denominator, which is also the HXF rule in equation 6. Recall that the X factor (XF) is a semiconductor industry jargon describing the ratio of the accumulated flow time in the system over the sum of the processing time of the operations completed. Thus, the lots that are lagging behind relative to their theoretical processing time are expedited. Now, if we consider  $\text{Wt}(\text{PT} + \text{WINQ})/\text{XF}$ , in order to see the composite building blocks, equation 13 may be shown in attribute abbreviated terms, where the scaling parameters are highlighted:

$$\text{Wt}(\text{PT} + \text{WINQ})/\text{XF} = \mathbf{exp}(-\mathbf{XF}) \cdot \left( \frac{\text{PT} + \text{WINQ}}{\text{XF}} \right) + \mathbf{exp}(\mathbf{XF}) \cdot \left( \frac{1}{\text{XF}} \right) \quad (15)$$

This new rule introduced XF, as a priority index building block; and as a dynamic scaling parameter. System-based scaling parameters eliminate trial-and-error simulation to find the weight of the parameters (Ovacik and Uzsoy 1994). For instance, Raghu and Rajendran (1993) weighed the processing time and the due-date attributes as a function of machine utilisation ( $\eta$ ):

$$RR_{ij} = \left( \frac{d_i - t - \sum_{q=j}^{m_i} P_{iq}}{\left( \sum_{q=j}^{m_i} P_{iq} \right)} \right) (\exp(-\eta)p_{ij} + \exp(\eta)p_{ij} + W_{i(j+1)}) \quad (16)$$

In our new rules, key lot and fab status attributes such as PT and WINQ are weighed based on how the lot is faring for its flow time relative to its processing time (XF).  $Wt(PT + WINQ)/XF$  expedites lots with the least sum of  $(PT + WINQ)/XF$  and  $1/XF$ . Further, the greater the XF, the greater the weight of the  $(1/XF)$  component. Stated otherwise, PT and WINQ, are given less weight when the lot lags behind its processing time. Other comments on the dispatching rules used include the critical ratio (CR) rule (equation 5) which is common in semiconductor fabs, and which is the ratio of the remaining processing time and remaining time until the due date. Finally,  $Wt(ATStep-RPT)/XF$  blended  $(ATStep-RPT)/XF$  into  $Wt(PT + WINQ)/XF$ , to improve flow time variance performance.

**4.1.2 Input regulation.** In CONWIP, separate fixed-WIP levels were set for each product. In each fab, the average product-specific WIP levels recorded as dependent variables under push and FCFS, were re-used in CONWIP as independent variables. The push-FCFS WIP levels were used across the rest of the dispatching rules because we wanted to reduce this experiment's number of factors.

**4.1.3 Number of products/production mode.** The number-of-products (or fab type) factor addresses whether make-to-order (high mix and low volume (ASIC)) and make-to-market (low mix and high volume) production modes affect dispatching and lot release performance. In order to have the factory be the controlled variable, we selected a single fab, fixed all its operating characteristics, and only varied the number of products, by releasing a fraction of the original ASIC products, and increasing the individual product release rates, as to end up with the same overall throughput rate in both fabs. For the low-variety level, 3 products were chosen as to have similar tool utilisation levels as in the original 21-product case.

## 4.2 Experimental test bed

SEMATECH set 5 (Feigin *et al.* 1994) described an anonymous fab's flow data such as product routings, processing times, and equipment/operator availability. It was downloaded via ftp from the Arizona State University *Modeling and Analysis for Semiconductor Manufacturing* laboratory site ([www.eas.asu.edu/~masmlab](http://www.eas.asu.edu/~masmlab)). Its characteristics are summarised in table 4.

Table 4. Key characteristics of SEMATECH Set 5 (Feigin *et al.* 1994) as modeled in this study.

Modeling aspect	Set 5 [31]
Product type	ASIC
Number of products	21
Number of routes	14
Lot wafer size	25, 50
Average number of process steps per layer	30
Number of work centers (tool groups)	85
Number of identical machines per work center	1–9
Operators modeled?	Yes
Rework modeled?	No
Yield loss (scrap) modeled?	No
Automated material handling or travel time	No
Wafer starts per month (approximately)	10,000
Raw process time range (hours)	172–368
Number of processing steps range	117–259
Total number of processing steps	3824
Preventive maintenance included?	Yes
Batching policy	MBS (greedy)
Group set-up modeled?	No
Job type set-up modeled?	Yes
Processing time distributions	Constant
Load and unload time distributions	Constant
Setup time distributions	Constant
MTTF distributions	Exponential
MTTR distributions	Exponential

### 4.3 Simulation procedure

AutoSched AP 6.25 was the software package used, along with C++ customisation for some dispatching rules. Model validation used the sample run data in Feigin *et al.* (1994). The replication-deletion method (Law and Kelton 1991) was used to reproduce point estimates and 95% confidence intervals for the studied response measures. This approach involved running 10 independent replications for each level of the  $2 \times 2 \times 14$  factorial experiment for 5 years, and discarding the first year as initial transient statistics from each replication. Tool reliability was the main factor behind variability, and different random stream seed increments were used in each treatment level. Also note that including batching, set-ups, operator resources, and re-entrant flow sets this study apart from typical job shop studies.

### 4.4 Due-date tightness

Due-date tightness was a fixed factor in this study. The total work content method was used to assign each lot released into the fab a due date based on twice its total processing time. Note that only EDD, CR, and CR + SPT incorporated due-date information.

Table 5. Description of relevant performance measures.

Performance measure	Description
Average WIP level (WIPAVG)	Average number of lots present in the fab during the non-transient run time period
Mean flow time (MFT)	Average time a lot spends in the fab from release to completion
Standard deviation of flow time (SDFT) 98% cycle time (98% CT)	Standard deviation of flow time MFT + 3 SDFT (Industry jargon with no relation to the central limit theorem)
Percentage of tardy lots (%Tardy)	Percentage of the lots which were completed past their respective due-dates
Mean conditional tardiness (MCT) % over FCFS	Average time a lot is past due, if late Rule's improvement in percentage terms over FCFS under the same release mechanism
95% confidence interval ( $\pm$ CI)	Confidence interval

#### 4.5 Statistical analysis methodology

Using SAS 8.0, our analysis referred to 1, 2, and 3-way ANOVAs, and hypothesis tests for relevant factors at stake. These were followed by the Ryan multiple comparison procedure (MCP) to rank the factor levels. The response variables collected in this study are listed and defined in table 5. When ANOVA concludes that a factor has a significant effect on a response variable, it does not rank the factor levels in order of best performance. Multiple comparison procedures can be employed to rank the flow control strategies. Like the often-used Tukey procedure, the Ryan MCP uses pair-wise comparisons based on a studentised range distribution, and was recommended by Toothhaker (1991) for its general-purpose power and versatility.

### 5. Results and discussion

#### 5.1 Experimental results

System-oriented performance measures such as mean and standard deviation of flow time are the focus of this section, given their primordial importance in the semiconductor manufacturing context. Due-date adherence measures are reported as secondary. When looking at tables 6 and 7, note that the performance of dispatching rules is compared alongside the benchmark FCFS performance in the column under '% over FCFS'. Since this is meant to relay the rule's improvement over FCFS, a positive percentage value refers to a decrease in the flow time measure considered.

Table 6 confirms Little's law in the push case, as smaller average WIP levels matched shorter MFT. Our proposed rules showed 2% MFT improvements over FCFS. As for SDFT, 50% and 25% improvements over FCFS were respectively achieved by AT-RPT and (ATStep-RPT)/XF; in the three- and 21-product cases. The throughput fluctuation seen under CONWIP was caused by generalising FCFS fixed-WIP levels across the rest of the rules as described in section 4.1.2. Even though, compared with push, pull performance deteriorated for most rules other

Table 6. Experimental results from the push and CONWIP cases.

Push	No. of Products	Dispatching Rule	WIPAVG		MFT		SDFT		98% CT		
			lots ( $\pm$ CI)	hours ( $\pm$ CI)	hours ( $\pm$ CI)	%over FCFS	hours ( $\pm$ CI)	%over FCFS	hours	% over FCFS	
3	FCFS		168.2 ( $\pm$ 0.8)	444.6 ( $\pm$ 2.1)	—	41.2 ( $\pm$ 0.5)	—	568.1	—	—	
	EDD		175.9 ( $\pm$ 1.0)	465.0 ( $\pm$ 2.8)	-4.6%	60.8 ( $\pm$ 0.5)	-46.6%	647.1	-13.9%	-13.9%	
	CR		175.4 ( $\pm$ 0.8)	463.6 ( $\pm$ 2.1)	-4.2%	46.7 ( $\pm$ 1.1)	-13.3%	602.3	-6.0%	-6.0%	
	LWNQ		168.8 ( $\pm$ 0.5)	446.3 ( $\pm$ 1.4)	-0.2%	51.7 ( $\pm$ 0.8)	-25.5%	598.0	-5.3%	-5.3%	
	ESD		179.5 ( $\pm$ 0.7)	474.5 ( $\pm$ 1.8)	-6.7%	22.4 ( $\pm$ 0.7)	45.5%	541.9	4.6%	4.6%	
	HXF		165.0 ( $\pm$ 0.5)	436.1 ( $\pm$ 1.4)	1.9%	46.8 ( $\pm$ 0.3)	-13.8%	576.6	-1.5%	-1.5%	
	CR + SPT		171.7 ( $\pm$ 1.0)	454.0 ( $\pm$ 2.7)	-2.1%	64.6 ( $\pm$ 0.8)	-56.9%	647.8	-14.0%	-14.0%	
	AT-RPT		178.4 ( $\pm$ 0.9)	471.8 ( $\pm$ 2.5)	-6.1%	20.2 ( $\pm$ 0.8)	50.9%	532.4	6.3%	6.3%	
	PT/TIS		170.8 ( $\pm$ 0.9)	451.5 ( $\pm$ 2.4)	-1.6%	65.7 ( $\pm$ 1.2)	-59.6%	648.6	-14.2%	-14.2%	
	(PT + WINQ)/TIS		169.8 ( $\pm$ 0.7)	448.8 ( $\pm$ 1.9)	0.9%	49.8 ( $\pm$ 0.5)	-21.0%	676.4	-19.1%	-19.1%	
	(PT + WINQ)/XF		165.0 ( $\pm$ 0.8)	436.2 ( $\pm$ 2.0)	1.9%	60.2 ( $\pm$ 1.2)	-46.4%	617.0	-8.6%	-8.6%	
	(ATStep-RPT)/XF		165.5 ( $\pm$ 0.6)	437.6 ( $\pm$ 1.5)	1.6%	46.9 ( $\pm$ 0.5)	-13.8%	578.3	-1.8%	-1.8%	
	Wt(PT + WINQ)/XF		164.8 ( $\pm$ 0.4)	435.7 ( $\pm$ 1.1)	2.0%	53.7 ( $\pm$ 0.2)	-23.4%	596.8	-5.1%	-5.1%	
	Wt(ATStep-RPT)/XF		164.5 ( $\pm$ 0.6)	434.8 ( $\pm$ 1.5)	2.2%	51.2 ( $\pm$ 0.5)	-24.4%	588.4	-3.6%	-3.6%	
	21	FCFS		186.4 ( $\pm$ 0.9)	492.9 ( $\pm$ 2.4)	—	91.8 ( $\pm$ 2.7)	—	774.4	—	—
		EDD		194.2 ( $\pm$ 0.8)	513.4 ( $\pm$ 2.1)	-4.2%	97.5 ( $\pm$ 1.3)	-6.2%	806.0	-4.1%	-4.1%
		CR		196.3 ( $\pm$ 2.7)	519.2 ( $\pm$ 7.3)	-5.3%	88.6 ( $\pm$ 4.0)	3.6%	784.9	-1.4%	-1.4%
LWNQ			191.9 ( $\pm$ 1.4)	507.5 ( $\pm$ 3.6)	-3.0%	117.2 ( $\pm$ 5.9)	-27.6%	859.0	-10.9%	-10.9%	
ESD			195.6 ( $\pm$ 1.9)	517.2 ( $\pm$ 5.1)	-4.9%	74.7 ( $\pm$ 5.0)	18.6%	741.3	4.3%	4.3%	
HXF			186.7 ( $\pm$ 1.8)	493.7 ( $\pm$ 4.9)	-0.2%	73.5 ( $\pm$ 4.9)	19.9%	714.3	7.8%	7.8%	
CR + SPT			193.4 ( $\pm$ 1.2)	511.5 ( $\pm$ 3.2)	-3.8%	95.9 ( $\pm$ 1.6)	-4.4%	799.0	-3.2%	-3.2%	
AT-RPT			194.2 ( $\pm$ 1.7)	513.5 ( $\pm$ 4.5)	-4.2%	72.1 ( $\pm$ 4.9)	21.5%	729.9	5.8%	5.8%	
PT/TIS			191.3 ( $\pm$ 1.0)	505.8 ( $\pm$ 2.7)	-2.6%	92.7 ( $\pm$ 2.6)	-0.9%	783.8	-1.2%	-1.2%	
(PT + WINQ)/TIS			190.0 ( $\pm$ 1.4)	502.3 ( $\pm$ 3.6)	-1.9%	87.2 ( $\pm$ 3.6)	5.1%	763.9	1.4%	1.4%	
(PT + WINQ)/XF		185.9 ( $\pm$ 1.8)	491.6 ( $\pm$ 4.8)	0.3%	85.4 ( $\pm$ 4.7)	7.0%	747.9	3.4%	3.4%		
(ATStep-RPT)/XF		184.8 ( $\pm$ 1.5)	488.5 ( $\pm$ 4.0)	0.9%	69.1 ( $\pm$ 2.6)	24.7%	695.8	10.2%	10.2%		
Wt(PT + WINQ)/XF		182.9 ( $\pm$ 1.2)	483.7 ( $\pm$ 3.0)	1.9%	76.0 ( $\pm$ 2.2)	17.2%	711.7	8.1%	8.1%		
Wt(ATStep-RPT)/XF		182.8 ( $\pm$ 0.9)	483.2 ( $\pm$ 2.4)	2.0%	73.7 ( $\pm$ 2.0)	19.7%	704.4	9.0%	9.0%		

Pull (CONWIP)	3	FCFS	168	451.9 ( $\pm 1.0$ )	-	46.8 ( $\pm 0.8$ )	-120.0%	592.2	-		
		EDD	168	446.7 ( $\pm 1.4$ )	1.2%	102.9 ( $\pm 2.4$ )	-358.8%	755.3	-27.5%		
		CR	168	566.5 ( $\pm 4.1$ )	-25.4%	214.6 ( $\pm 4.8$ )	-	1210.2	-104.4%		
		LWNQ	168	452.8 ( $\pm 1.0$ )	-0.2%	61.1 ( $\pm 1.1$ )	-30.6%	636.0	-7.4%		
		ESD	168	451.7 ( $\pm 0.8$ )	0.1%	46.7 ( $\pm 0.9$ )	0.0%	591.9	0.1%		
		HXF	168	582.1 ( $\pm 7.4$ )	-28.8%	309.7 ( $\pm 6.5$ )	-562.2%	1511.1	-155.2%		
		CR+SPT	168	450.4 ( $\pm 1.5$ )	0.3%	90.6 ( $\pm 2.1$ )	-93.8%	722.3	-22.0%		
		AT-RPT	168	531.5 ( $\pm 40.0$ )	-17.6%	163.9 ( $\pm 36.3$ )	-250.5%	1023.2	-72.8%		
		PT/TIS	168	450.2 ( $\pm 2.1$ )	0.4%	114.8 ( $\pm 4.0$ )	-145.5%	794.7	-34.2%		
		(PT + WINQ)/TIS	168	450.3 ( $\pm 1.8$ )	0.4%	105.5 ( $\pm 3.0$ )	-125.6%	766.8	-29.5%		
		(PT + WINQ)/XF	168	467.3 ( $\pm 2.3$ )	-3.4%	152.0 ( $\pm 6.1$ )	-225.0%	923.2	-55.9%		
		(ATStep-RPT)/XF	168	583.0 ( $\pm 3.1$ )	-29.0%	298.4 ( $\pm 5.3$ )	-538.1%	1478.1	-149.6%		
		Wt(PT + WINQ)/XF	168	453.5 ( $\pm 1.2$ )	-0.4%	44.7 ( $\pm 0.9$ )	4.4%	587.7	0.8%		
		Wt(ATStep-RPT)/XF	168	577.8 ( $\pm 3.4$ )	-27.8%	287.8 ( $\pm 3.6$ )	-515.6%	1441.3	-143.4%		
		21		FCFS	186	495.8 ( $\pm 1.16$ )	-	90.2 ( $\pm 0.83$ )	-	766.4	-
				EDD	186	501.6 ( $\pm 0.81$ )	-1.2%	218.6 ( $\pm 4.40$ )	-142.3%	1157.3	-51.0%
				CR	186	602.2 ( $\pm 6.31$ )	-17.7%	229.9 ( $\pm 5.18$ )	-154.9%	1291.9	-68.6%
				LWNQ	186	498.0 ( $\pm 0.71$ )	-0.4%	104.8 ( $\pm 1.08$ )	-16.2%	812.4	-6.0%
				ESD	186	495.6 ( $\pm 0.41$ )	0.1%	90.8 ( $\pm 0.55$ )	-0.7%	768.0	-0.2%
				HXF	186	570.4 ( $\pm 4.32$ )	-15.0%	236.8 ( $\pm 4.49$ )	-162.5%	1280.8	-67.1%
				CR+SPT	186	512.7 ( $\pm 1.21$ )	-3.4%	138.6 ( $\pm 2.27$ )	-53.7%	928.5	-21.2%
AT-RPT	186			605.6 ( $\pm 2.93$ )	-22.1%	220.3 ( $\pm 6.52$ )	-144.3%	1266.6	-65.3%		
PT/TIS	186			512.0 ( $\pm 1.00$ )	-3.3%	187.5 ( $\pm 2.56$ )	-107.9%	1074.7	-40.2%		
(PT + WINQ)/TIS	186			511.8 ( $\pm 1.12$ )	-3.2%	174.6 ( $\pm 3.11$ )	-93.5%	1035.6	-35.1%		
(PT + WINQ)/XF	186			542.8 ( $\pm 2.70$ )	-9.5%	215.6 ( $\pm 4.37$ )	-139.1%	1189.6	-55.2%		
(ATStep-RPT)/XF	186			573.1 ( $\pm 6.98$ )	-15.6%	229.0 ( $\pm 6.57$ )	-153.9%	1260.1	-64.4%		
Wt(PT + WINQ)/XF	186			500.2 ( $\pm 0.75$ )	-0.9%	89.2 ( $\pm 0.44$ )	1.1%	767.8	-0.2%		
Wt(ATStep-RPT)/XF	186			560.7 ( $\pm 5.84$ )	-13.1%	221.5 ( $\pm 6.57$ )	-145.6%	1225.1	-59.8%		

Table 7. Experimental results for secondary performance measures for the push case.

	No. of Products	Dispatching Rule	% Tardy % ( $\pm$ CI)	MCT			
				hours ( $\pm$ CI)	% over FCFS		
Push	3	FCFS	0.02% ( $\pm$ 0.01)	9.6 ( $\pm$ 4.0)	–		
		EDD	0.01% ( $\pm$ 0.01)	6.4 ( $\pm$ 3.3)	33.7%		
		CR	0.2% ( $\pm$ 0.1)	6.5 ( $\pm$ 2.9)	33.0%		
		LWNQ	0.9% ( $\pm$ 0.2)	28.3 ( $\pm$ 2.8)	–193.0%		
		ESD	1.5% ( $\pm$ 0.6)	11.4 ( $\pm$ 2.0)	–18.3%		
		HXF	0%	0	100.0%		
		CR + SPT	0.1% ( $\pm$ 0.1)	6.9 ( $\pm$ 2.9)	28.2%		
		AT-RPT	1.7% ( $\pm$ 0.5)	11.6 ( $\pm$ 1.1)	–20.3%		
		PT/TIS	0.1% ( $\pm$ 0.1)	16.8 ( $\pm$ 8.1)	–74.4%		
		(PT + WINQ)/TIS	0.04% ( $\pm$ 0.03)	12.5 ( $\pm$ 4.9)	–29.2%		
		(PT + WINO)/XF	0%	0	100.0%		
		(ATStep-RPT)/XF	0%	0	100.0%		
		Wt(PT + WINO)/XF	0%	0	100.0%		
		Wt(ATStep-RPT)/XF	0%	0	100.0%		
			21	FCFS	10.3% ( $\pm$ 2.3)	23.9 ( $\pm$ 2.7)	–
				EDD	12.6% ( $\pm$ 1.1)	31.9 ( $\pm$ 1.6)	–33.2%
CR	14.9% ( $\pm$ 5.5)			17.3 ( $\pm$ 7.0)	27.7%		
LWNQ	19.0% ( $\pm$ 1.5)			83.1 ( $\pm$ 8.8)	–247.3%		
ESD	13.3% ( $\pm$ 3.8)			28.9 ( $\pm$ 7.9)	–20.9%		
HXF	3.0% ( $\pm$ 3.6)			13.2 ( $\pm$ 4.9)	45.0%		
CR + SPT	13.0% ( $\pm$ 3.6)			12.2 ( $\pm$ 3.0)	49.1%		
AT-RPT	11.8% ( $\pm$ 4.6)			22.3 ( $\pm$ 3.9)	6.8%		
PT/TIS	14.4% ( $\pm$ 1.5)			42.3 ( $\pm$ 2.6)	–76.7%		
(PT + WINQ)/TIS	11.2% ( $\pm$ 1.9)			41.0 ( $\pm$ 4.3)	–71.2%		
(PT + WINQ)/XF	5.5% ( $\pm$ 3.2)			20.1 ( $\pm$ 9.1)	16.0%		
(ATStep-RPT)/XF	0.7% ( $\pm$ 0.6)			9.9 ( $\pm$ 3.5)	58.6%		
Wt(PT + WINQ)/XF	0.8% ( $\pm$ 0.6)			9.3 ( $\pm$ 3.2)	61.1%		
Wt(ATStep-RPT)/XF	0.3% ( $\pm$ 0.2)			5.6 ( $\pm$ 2.0)	76.5%		

than FCFS, the proposed Wt(PT + WINQ)/XF was robustly competitive *vis-à-vis* FCFS in CONWIP, especially when considering the 98% cycle time measure. Finally, our proposed rules substantially improved due-date adherence in both fabs under fixed-interval push release (table 7).

## 5.2 Analysis of variance and Ryan mean comparison procedure results

The three-way analysis of variance factors (number of products (NP), order release (OR), and dispatching (DR)) and their interactions; significantly affected MFT and SDFT. This was followed by relevant two-way ANOVAs (DR  $\times$  OR) for each and both fabs combined; and one-way ANOVAs (DR) for combinations of (OR  $\times$  NP). As the null hypothesis for equality of means was rejected at the 5% significance level for all the ANOVAs, Ryan MCP tables will be the focus of this section. Contrary to tables 6 and 7, the factors are ranked with the best levels at the top of the MCP tables. They are also grouped as indicated by adjacent vertical lines.

Tables 8 and 9 show the ranking of order release and dispatching rule pairs for the two factory types. In the 21-product fab, Wt(PT + WINQ)/XF and

Table 8. Ryan MCP ranking for the (OR  $\times$  DR) factor: 21-product fab.

		MFT				SDFT	
(OR $\times$ DR)		(hours)		(OR $\times$ DR)		(hours)	
Push	x	Wt(ATStep-RPT)/XF	483.2	Push	x	(ATStep-RPT)/XF	69.1
Push	x	Wt(PT+WINQ)/XF	483.7	Push	x	AT-RPT	72.1
Push	x	(ATStep-RPT)/XF	488.5	Push	x	HXF	73.5
Push	x	(PT+WINQ)/XF	491.6	Push	x	Wt(ATStep-RPT)/XF	73.7
Push	x	FCFS	492.9	Push	x	ESD	74.7
Push	x	HXF	493.7	Push	x	Wt(PT+WINQ)/XF	76.0
CONWIP	x	ESD	495.6	Push	x	(PT+WINQ)/XF	85.5
CONWIP	x	FCFS	495.9	Push	x	(PT+WINQ)/TIS	87.2
CONWIP	x	LWNQ	498.0	Push	x	CR	88.6
CONWIP	x	Wt(PT+WINQ)/XF	500.2	CONWIP	x	Wt(PT+WINQ)/XF	89.2
CONWIP	x	EDD	501.6	CONWIP	x	FCFS	90.2
Push	x	(PT+WINQ)/TIS	502.3	CONWIP	x	ESD	90.8
Push	x	PT/TIS	505.8	Push	x	FCFS	91.8
Push	x	LWNQ	507.5	Push	x	PT/TIS	92.7
Push	x	CR+SPT	511.5	Push	x	CR+SPT	95.9
CONWIP	x	(PT+WINQ)/TIS	511.8	Push	x	EDD	97.5
CONWIP	x	PT/TIS	512.0	CONWIP	x	LWNQ	104.8
CONWIP	x	CR+SPT	512.7	Push	x	LWNQ	117.2
Push	x	EDD	513.4	CONWIP	x	CR+SPT	138.6
Push	x	AT-RPT	513.5	CONWIP	x	(PT+WINQ)/TIS	174.6
Push	x	ESD	517.2	CONWIP	x	PT/TIS	187.5
Push	x	CR	519.2	CONWIP	x	(PT+WINQ)/XF	215.6
CONWIP	x	(PT+WINQ)/XF	542.8	CONWIP	x	EDD	218.6
CONWIP	x	Wt(ATStep-RPT)/XF	560.7	CONWIP	x	AT-RPT	220.3
CONWIP	x	HXF	570.4	CONWIP	x	Wt(ATStep-RPT)/XF	221.5
CONWIP	x	(ATStep-RPT)/XF	573.1	CONWIP	x	(ATStep-RPT)/XF	229.0
CONWIP	x	CR	602.2	CONWIP	x	CR	229.9
CONWIP	x	AT-RPT	605.6	CONWIP	x	HXF	236.8

Wt(ATStep-RPT)/XF under push, were best for MFT, while being distinctly superior from the (Push  $\times$  FCFS) pair. Wt(PT + WINQ)/XF was also robust under pull. FCFS, PT/TIS, and especially CR + SPT were insensitive to OR. Except for EDD, ESD, and LWNQ, dispatching rules fared better under push. As for SDFT, ESD, HXF, AT-RPT, (ATStep-RPT)/XF, Wt(PT + WINQ)/XF, and Wt(ATStep-RPT)/XF, all under push; were best. Further, CONWIP only benefited LWNQ. Best SDFT performers such as AT-RPT, (ATStep-RPT)/XF, HXF, and Wt(ATStep-RPT)/XF deteriorated under pull.

In the three-product fab, there is more group overlap for MFT (table 9). The best combinations (Push  $\times$  Wt(ATStep-RPT)/XF) and (Push  $\times$  Wt(PT + WINQ)/XF), were also in the same group as 14 other pairs. Pull and push pairs of CR + SPT, LWNQ, FCFS, PT/TIS, (PT + WINQ)/TIS were not statistically different. Only EDD and ESD statistically improved from push to pull. Contrary to the 21-product ASIC fab, we can notice a better pull performance, but without statistically improving any rule over push. As for SDFT, the best group was made of (Push  $\times$  ESD) and (Push  $\times$  AT-RPT). FCFS, LWNQ, and Wt(PT + WINQ)/XF were statistically insensitive to OR; and HXF, AT-RPT, (ATStep-RPT)/XF, and CR were dramatically eroded by pull.

Table 10 ranks the individual dispatching rules for each of the four order release and factory type combinations. In the 21-product fab under push, (ATStep-RPT)/XF and Wt(PT + WINQ)/XF were the best for both MFT and SDFT while being distinct from FCFS. The same performance was seen for MCT and %Tardy (table 11), where due-date-based rules such as EDD, were no match to the proposed rules. In the three-product fab under push, despite more group separation, 21-product fab trends were seen for MFT, with the top rules of Wt(PT + WINQ)/XF and (ATStep-RPT)/XF, being joined by HXT, (PT + WINQ)/XT, and

Table 9. Ryan MCP ranking for the (OR  $\times$  DR) factor: 3-product fab.

MFT			SDFT				
(OR $\times$ DR)		(hours)	(OR $\times$ DR)		(hours)		
Push	x	Wt(ATStep-RPT)/XF	434.8	Push	x	AT-RPT	20.2
Push	x	Wt(PT+WINQ)/XF	435.7	Push	x	ESD	22.5
Push	x	HXF	436.1	Push	x	FCFS	41.2
Push	x	(PT+WINQ)/XF	436.2	CONWIP	x	Wt(PT+WINQ)/XF	44.7
Push	x	(ATStep-RPT)/XF	437.7	Push	x	CR	46.7
Push	x	FCFS	444.6	CONWIP	x	ESD	46.8
Push	x	LWNQ	446.3	CONWIP	x	FCFS	46.8
CONWIP	x	EDD	446.7	Push	x	HXF	46.8
Push	x	(PT+WINQ)/TIS	448.8	Push	x	(ATStep-RPT)/XF	46.9
CONWIP	x	PT/TIS	450.3	Push	x	(PT+WINQ)/TIS	49.8
CONWIP	x	(PT+WINQ)/TIS	450.3	Push	x	Wt(ATStep-RPT)/XF	51.2
CONWIP	x	CR+SPT	450.4	Push	x	LWNQ	51.7
Push	x	PT/TIS	451.5	Push	x	Wt(PT+WINQ)/XF	53.7
CONWIP	x	ESD	451.7	Push	x	(PT+WINQ)/XF	60.3
CONWIP	x	FCFS	451.9	Push	x	EDD	60.8
CONWIP	x	LWNQ	452.8	CONWIP	x	LWNQ	61.1
CONWIP	x	Wt(PT+WINQ)/XF	453.5	Push	x	CR+SPT	64.6
Push	x	CR+SPT	454.0	Push	x	PT/TIS	65.7
Push	x	CR	463.6	CONWIP	x	CR+SPT	90.6
Push	x	EDD	465.0	CONWIP	x	EDD	102.9
CONWIP	x	(PT+WINQ)/XF	467.3	CONWIP	x	(PT+WINQ)/TIS	105.5
Push	x	AT-RPT	471.8	CONWIP	x	PT/TIS	114.8
Push	x	ESD	474.5	CONWIP	x	(PT+WINQ)/XF	152.0
CONWIP	x	AT-RPT	531.5	CONWIP	x	AT-RPT	163.9
CONWIP	x	CR	566.5	CONWIP	x	CR	214.6
CONWIP	x	Wt(ATStep-RPT)/XF	577.8	CONWIP	x	Wt(ATStep-RPT)/XF	287.8
CONWIP	x	HXF	582.1	CONWIP	x	(ATStep-RPT)/XF	298.4
CONWIP	x	(ATStep-RPT)/XF	583.0	CONWIP	x	HXF	309.7

Wt(ATStep-RPT)/XF. In contrast, SDFT was dominated by AT-RPT. Table 11 again confirmed the superiority of our new rules for the due-date measures in the three-product case. In the 21-product fab under pull, top MFT rules were such for SDFT as well: FCFS, ESD, and Wt(PT + WINQ)/XF. LWNQ was in the best performing MFT group and was in the second best group for SDCT. HXF, CR, and (ATStep-RPT)/XF lagged in both MCT and SDCT. In the three-product fab under pull, the best rules for both SDCT and MCT were FCFS, ESD, Wt(PT + WINQ)/XF, and LWNQ. As in the 21-product fab, HXF, (ATStep-RPT)/XF, Wt(ATStep-RPT)/XF, and CR were poor for both MCT and SDCT.

### 5.3 The 98% cycle time performance measure

We recorded the semiconductor industry's own '98% cycle time' measure, with the actual 98th percentile mean flow time (table 12). Recall that the former is defined as the mean plus three standard deviations of flow time. The latter's value was found by merging flow time values from 10 replications, sorting them in ascending order, and finding the 98th percentile value. The 98% cycle time value overestimated the 98th percentile mean flow time by about 15%.

## 6. Conclusions

### 6.1 Summary

We have assembled a group of current and benchmark dispatching rules, and compared them alongside the rules that we propose. We have conducted rigorous simulation and statistical analyses on a realistic semiconductor test bed factory.

Table 10. Ryan MCP ranking for the DR factor under the four (OR  $\times$  NP) combinations.

No. of Products	MFT		SDFT			
	(Dispatching rule)	(hours)	(Dispatching rule)	(hours)		
Push	3	Wt(ATStep-RPT)/XF	434.8	AT-RPT	20.2	
		Wt(PT+WINQ)/XF	435.7	ESD	22.5	
		HXF	436.1	FCFS	41.2	
	21	(PT+WINQ)/XF	436.2	CR	46.7	
		(ATStep-RPT)/XF	437.7	HXF	46.8	
		FCFS	444.6	(ATStep-RPT)/XF	46.9	
		LWNQ	446.3	(PT+WINQ)/TIS	49.8	
		(PT+WINQ)/TIS	448.8	Wt(ATStep-RPT)/XF	51.2	
		PT/TIS	451.5	LWNQ	51.7	
		CR+SPT	454.0	Wt(PT+WINQ)/XF	53.7	
		CR	463.6	(PT+WINQ)/XF	60.3	
		EDD	465.0	EDD	60.8	
		AT-RPT	471.8	CR+SPT	64.6	
		ESD	474.5	PT/TIS	65.7	
		3	Wt(ATStep-RPT)/XF	483.2	(ATStep-RPT)/XF	69.1
			Wt(PT+WINQ)/XF	483.7	AT-RPT	72.1
			(ATStep-RPT)/XF	488.5	HXF	73.5
			(PT+WINQ)/XF	491.6	Wt(ATStep-RPT)/XF	73.7
			FCFS	492.9	ESD	74.7
			HXF	493.7	Wt(PT+WINQ)/XF	76.0
			(PT+WINQ)/TIS	502.3	(PT+WINQ)/XF	85.5
PT/TIS	505.8		(PT+WINQ)/TIS	87.2		
LWNQ	507.5		CR	88.6		
CR+SPT	511.5		FCFS	91.8		
EDD	513.4		PT/TIS	92.7		
AT-RPT	513.5		CR+SPT	95.9		
ESD	517.2		EDD	97.5		
CR	519.2		LWNQ	117.2		
Pull (CONWIP)	3		EDD	446.7	Wt(PT+WINQ)/XF	44.7
		PT/TIS	450.3	ESD	46.8	
		(PT+WINQ)/TIS	450.3	FCFS	46.8	
	21	CR+SPT	450.4	LWNQ	61.1	
		ESD	451.7	CR+SPT	90.6	
		FCFS	451.9	EDD	102.9	
		LWNQ	452.8	(PT+WINQ)/TIS	105.5	
		Wt(PT+WINQ)/XF	453.5	PT/TIS	114.8	
		(PT+WINQ)/XF	467.3	(PT+WINQ)/XF	152.0	
		AT-RPT	531.5	AT-RPT	163.9	
		CR	566.5	CR	214.6	
		Wt(ATStep-RPT)/XF	577.8	Wt(ATStep-RPT)/XF	287.8	
		HXF	582.1	(ATStep-RPT)/XF	298.4	
		(ATStep-RPT)/XF	583.0	HXF	309.7	
		21	ESD	495.6	Wt(PT+WINQ)/XF	89.2
FCFS	495.9		FCFS	90.2		
LWNQ	498.0		ESD	90.8		
Wt(PT+WINQ)/XF	500.2		LWNQ	104.8		
EDD	501.6		CR+SPT	138.6		
(PT+WINQ)/TIS	511.8		(PT+WINQ)/TIS	174.6		
PT/TIS	512.0		PT/TIS	187.5		
CR+SPT	512.7		(PT+WINQ)/XF	215.6		
(PT+WINQ)/XF	542.8		EDD	218.6		
Wt(ATStep-RPT)/XF	560.7		AT-RPT	220.3		
HXF	570.4		Wt(ATStep-RPT)/XF	221.5		
(ATStep-RPT)/XF	573.1		(ATStep-RPT)/XF	229.0		
CR	602.2		CR	229.9		
AT-RPT	605.6		HXF	236.8		

We have also identified robust dispatching rule and order release combinations for both production modes. The principal finding of this work, however, is that a proposed rule Wt(PT + WINQ)/XF, achieved superior results for multiple objectives spanning from mean and variance of flow time to due-date adherence performance measures. This rule was also robust under both order release strategies and both

Table 11. Ryan MCP ranking for the DR factor under two (OR  $\times$  NP) combinations (secondary performance measures).

No. of Products	MCT		%Tardy	
	(Dispatching rule)	(hours)	(Dispatching rule)	(%)
3	Wt(PT+WINQ)/XF	0.0	Wt(PT+WINQ)/XF	0.00
	ATStep-RPT)/XF	0.0	ATStep-RPT)/XF	0.00
	(PT+WINQ)/XF	0.0	(PT+WINQ)/XF	0.00
	Wt(ATStep-RPT)/XF	0.0	Wt(ATStep-RPT)/XF	0.00
	HXF	0.0	HXF	0.00
	EDD	3.2	EDD	0.01
	CR	6.5	FCFS	0.02
	CR+SPT	6.9	(PT+WINQ)/TIS	0.04
	FCFS	9.7	CR+SPT	0.06
	(PT+WINQ)/TIS	10.0	PT/TIS	0.13
	ESD	11.4	CR	0.16
	AT-RPT	11.6	LWNQ	0.90
	PT/TIS	16.8	ESD	1.52
	LWNQ	28.3	AT-RPT	1.67
21	Wt(ATStep-RPT)/XF	5.6	Wt(ATStep-RPT)/XF	0.32
	Wt(PT+WINQ)/XF	9.3	ATStep-RPT)/XF	0.70
	(ATStep-RPT)/XF	9.9	Wt(PT+WINQ)/XF	0.77
	CR+SPT	12.2	HXF	3.01
	HXF	13.2	(PT+WINQ)/XF	5.53
	CR	17.1	FCFS	10.29
	(PT+WINQ)/XF	20.1	(PT+WINQ)/TIS	11.22
	AT-RPT	22.3	AT-RPT	11.75
	FCFS	23.9	EDD	12.62
	ESD	28.9	CR+SPT	13.03
	EDD	31.9	ESD	13.36
	(PT+WINQ)/TIS	41.0	PT/TIS	14.41
	PT/TIS	42.3	CR	15.61
	LWNQ	83.1	LWNQ	19.02

Table 12. 98% cycle time versus 98th percentile of flow time.

<i>Experimental assumptions and results</i>	
Release policy	Push
Number of products	21
Dispatching rule	FCFS
Run Length (years)	5
Warm-up (years)	1
Number of independent replications	10
Mean cycle time (hours)	492.9 ( $\pm 2.4$ )
Standard deviation of cycle time (hours)	91.8 ( $\pm 2.7$ )
98% cycle time (hours)	768.4
98th percentile of cycle time (hours)	662.2

production modes. Researchers and practitioners are invited to test this dispatching rule in more factory settings.

Table 13 lists the best rules for MFT and SDFT, for combinations of production modes and order release. Wt(PT + WINQ)/XF was the most versatile of the 14 rules tested. The simpler (ATStep-RPT)/XF also achieved excellent dual results for MFT and SDFT, even though it was less robust under pull. Both rules were also in the best groups for MCT and %Tardy (table 14).

Table 13. Best rules for flow time measures.

Factory type $\times$ release policy	MFT	SDFt
21-product $\times$ CONWIP	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , FCFS, ESD, LWNQ, EDD	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , FCFS, ESD
3-product $\times$ CONWIP	(PT + WINQ)/TIS, (PT + WINQ)/XF, PT/TIS, CR + SPT, AT-RPT	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , FCFS, ESD, LWNQ
21-product $\times$ Push	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , (ATStep-RPT)/XF, $Wt(\text{ATStep-RPT})/\mathbf{XF}$	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , (ATStep-RPT)/XF, $Wt(\text{ATStep-RPT})/\mathbf{XF}$ , AT-RPT
3-product $\times$ Push	$Wt(\mathbf{PT} + \mathbf{WINQ})/\mathbf{XF}$ , (ATStep-RPT)/XF, $Wt(\text{ATStep-RPT})/\mathbf{XF}$ , (PT + WINQ)/XF, HXF	

Table 14. Best rules for due-date measures.

Factory type × release policy	MCT	% Tardy
21-product × Push	$W_t(\text{PT} + \text{WINQ})/\text{XF}, (\text{ATStep-RPT})/\text{XF},$ $W_t(\text{ATStep-RPT})/\text{XF}, \text{HXF}, \text{CR} + \text{SPT}$	$W_t(\text{PT} + \text{WINQ})/\text{XF}, (\text{ATStep-RPT})/\text{XF},$ $W_t(\text{ATStep-RPT})/\text{XF}, \text{HXF}, (\text{PT} + \text{WINQ})/\text{XF}$
3-product × Push	$W_t(\text{PT} + \text{WINQ})/\text{XF}, (\text{ATStep-RPT})/\text{XF},$ $W_t(\text{ATStep-RPT})/\text{XF}, \text{HXF}, (\text{PT} + \text{WINQ})/\text{XF}$	$W_t(\text{PT} + \text{WINQ})/\text{XF}, (\text{ATStep-RPT})/\text{XF},$ $W_t(\text{ATStep-RPT})/\text{XF}, \text{HXF}, (\text{PT} + \text{WINQ})/\text{XF}$

## 6.2 Past research retrospective

AT-RPT (Lu *et al.* (1994) and Holthaus 1999) and ESD confirmed their SDFT vocation. However,  $Wt(PT + WINQ)/XF$  broke their monopoly. LWNQ and similar WIP-balancing rules of Chevalier and Wein (1993), may only be recommended under pull policies. PT/TIS and  $(PT + WINQ)/TIS$  were proposed by Holthaus (1999) to dually address MFT and SDFT. Their performance however, was mid-range. No due-date based rule (CR, CR + SPT, EDD) outpaced FCFS for MFT or SDFT. This contrasts the reported extensive usage of CR in fabs by Mosley *et al.* (1998), Rippenhagen and Krishnaswamy (1998), and Johal (1998); even though, its performance might improve under loose due dates, and/or lighter loading levels. Lu *et al.* (1994) found that CONWIP lessened the effect of dispatching on MFT. We found that the benefits of including certain lot or fab-status attributes are mostly applicable in the push case. In fact, the good performance of the EDD and ESD under CONWIP for MFT, run counter to the way we understood the basics of composite rule design.

## 6.3 Contributions of this work

This work bridged between semiconductor flow control concepts (e.g. multiplier of theoretical flow time (XF) attribute and 98% cycle time measure), and ideas from the job shop control literature (e.g. scaling parameters in composite dispatching rule design and due-date adherence measures). Besides rigorous fab modelling and statistical analysis, composite rule design trends were adapted to the fab context. Original use of the multiplier of theoretical flow time (XF) as a priority index attribute and dynamic system-based scaling parameter; resulted in new versatile rules for the multiple objectives of MFT, SDFT, MCT, and %Tardy. Achieving a dual objective for just MFT and SDFT is not easy, as some researchers like Lu *et al.* (1994) custom-designed separate rules for each measure.

Push outperformed CONWIP in both the original ASIC fab (for MFT and SDFT), and the three-product fab (for SDFT). As for MFT in the three-product fab, pull improved for a tie with push. Up to this study, the effect of dispatching rules on CONWIP was not fully understood. In general, most rules failed to outpace FCFS in CONWIP, thus supporting the FCFS recommendation of Hopp and Spearman (1996). FCFS was also particularly insensitive to OR. Finally, the few available CONWIP studies for multiple products used a single factory-wide WIP-level, and careful sequencing of the released product types (Hopp and Roof 1998). Building on the ideas in Duenyas (1994), we also explored a product-specific WIP implementation in a large, unreliable, and batching-prone re-entrant fab.

## 6.4 Recommendations for future research

We reiterate our invitation for researchers inside and outside the semiconductor manufacturing field to further test some of the proposed dispatching rules. Further tests in fabs and job shops, will likely confirm the potential of the new rules. Batching policy and due date tightness can be added as experimental factors. Future research may also explore the effect of routing and priority attributes on separate product performance. In implementing CONWIP, one can either look at using fab-wide WIP

levels, or the optimisation of separate product WIP levels. In composite rule design, XF was encouraging as a dynamic scaling parameter, and should be further explored in job shop environments. Further, PT and WINQ can be respectively substituted by total remaining processing time (RPT), and total work content in all downstream queues; to make new composite dispatching rules.

### Acknowledgments

This work was supported in part by Daifuku Co., Ltd., Komaki, Aichi, Japan and AutoSimulations Inc., Bountiful, UT 84010, USA and was conducted while both authors were with the Industrial and Manufacturing Systems Engineering Department, Louisiana State University, Baton Rouge, LA 70802, USA.

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